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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,965	12/29/2003	Kaladhar Radhakrishnan	42P18282	9014

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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
VIGUSHIN, JOHN B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,965	RADHAKRISHNAN ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5,7,19 and 20* is/are allowed.

6)☒ Claim(s) *6,10,14 and 15* is/are rejected.

7)☒ Claim(s) *8,9,11-13 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed October 31, 2006. The Examiner acknowledges the amendments to Claims 6 and 15, and the addition of new Claims 19 and 20. Accordingly, Claims 1-20 are pending in the instant amended Application.

Rejections Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Hernandez (US Re. 35,064)† Kitamura et al. (US 5,095,626)

†Previously made of record by the Examiner in the Office Action of December 15, 2005.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6, 10, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hernandez. [*Examiner's Note*: Kitamura et al. is used as evidence, as explained in the rejections below, in accordance with multiple reference rejections under 35 USC § 102 set forth in the MPEP § 2131.01, part III].

As to Claim 6, Hernandez discloses, in Figs. 6 and 9-12, an integrated circuit (IC) coupled to a first side of an IC package (the IC and IC package contents of the dual in-line IC package 110, not shown, but inherently is present as the structural feature of this type of dual in-line package; col.6: 51-54);† and an array capacitor 90 (comprising the array of capacitor chips 102; col.6: 2-24; col.5: 33-37) attached to a second side of the IC package underneath the integrated circuit (Fig. 11), the capacitor 90 having openings 114 to enable pins 112 from the IC package to pass through (Fig. 11; col.6: 47-58).

†[*Examiner's Note*: Kitamura et al. discloses a dual in-line IC package of the type disclosed in Hernandez and is used as evidence that a dual in-line IC package of the type disclosed in Hernandez comprises an IC mounted on an IC package that carries the IC and leads, in accordance with the practice of multiple reference rejections under 35 USC § 102 set forth in the MPEP § 2131.01, part III]. Hernandez discloses a dual in-line IC package 110 but does not show its constituent parts. Kitamura et al. discloses, in Fig. 17 and col.14: 33-47, the constituent parts of a dual in-line IC package, of the type disclosed in Hernandez, which include an IC 42 and an IC package that carries the IC 42 and leads 46. Thus, the dual in-line IC package 110 of Hernandez inherently comprises an IC and an IC package that carries the IC and the leads 112, as in the dual in-line IC package 41 of Kitamura et al.

As to Claim 10, Hernandez discloses each of the openings 114 formed in the capacitor 90 has a diameter which is greater than a diameter of each pin 112 from the IC package such that a defined distance is maintained between an edge of each respective opening 114 and each respective pin 112 (Fig. 11).

As to Claim 14, the integrated circuit is embodied in a form of a semiconductor die (not shown, but inherently a structural constituent of the dual in-line package 110 of Hernandez, as shown in Kitamura et al. who provides the evidence, in Fig. 17 and col.14: 38-40, that in the dual in-line package of the type taught in Hernandez, the IC is embodied in a form of a semiconductor die 42. [*Examiner's Note*: This rejection is in accordance with the multiple reference rejections under 35 USC § 102 set forth in the MPEP 2131.01, part III].

As to Claim 15, Hernandez discloses, in Figs. 6 and 9-12, providing an array capacitor 90 (comprising the array of capacitor chips 102; col.6: 2-24; col.5: 33-37) with a plurality of openings 114 (Fig. 11; col.6: 51-58); providing an IC housed by an IC package;† passing pins from the IC package through the openings formed in the capacitor 90 (Fig. 11; col.6: 51-54); positioning the capacitor 90 on a backside of the IC package directly underneath the integrated circuit (Fig. 11); electrically connecting and attaching conductive terminals 98 between the capacitor 90 and the IC package (Figs. 9, 10 and 11; col.6: 51-58).

†[*Examiner's Note*: Kitamura et al. discloses a dual in-line IC package of the type disclosed in Hernandez and is used as evidence that a dual in-line IC package of the type disclosed in Hernandez comprises an IC mounted on an IC package that carries the IC and leads, in accordance with the practice of multiple reference rejections under 35 USC § 102 set forth in the MPEP § 2131.01, part III]. Hernandez discloses a dual in-line IC package 110 but does not show its constituent parts. Kitamura et al. discloses, in Fig. 17 and col.14: 33-47, the constituent parts of a dual in-line IC package, of the type disclosed in Hernandez, which include an IC 42 and an IC package that carries the IC 42 and leads 46. Thus, the dual in-line IC package 110 of Hernandez inherently comprises an IC

and an IC package that carries the IC and the leads 112, as in the dual in-line IC package 41 of Kitamura et al.

Allowable Subject Matter

5. Claims 1-5, 7, 19 and 20 have been allowed.

6. Claims 8, 9, 11-13 and 16-18 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-1984. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
December 03, 2006